INFORMATION CITED BY APPLICANTS THAT MAY BE MATERIAL TO THE PROSECUTION OF THE SUBJECT APPLICATION

Applicants: Y. Arima et al. Attorney Docket No. SUSU121795

Application No.: 10/674,951 Group Art Unit: 2811

Filed: September 30, 2003

Title: INTEGRATED CIRCUIT DEVICE

FOREIGN PATENT DOCUMENTS

*Examiner Initial	Cite No.	Document No.	Kind Code	Publication Date (mm/dd/yyyy)	Country	English Abstract Provided	English Translation Provided
	F1	10-78836	A	03/24/1998	Japan		
	F2	2000-82014	A	03/21/2000	Japan		

OTHER INFORMATION
(Including Author, Title, Date, Pertinent Pages, Etc.)

*Examiner Initial	Cite No.	
	O1	Kosonocky, S.V., et al., "Enhanced Multi-Threshold (MTCMOS) Circuits Using Variable Well Bias," *The International Symposium on Low Power Electronics and Design 2001*, Huntington Beach, California, August 6-7, 2001, pp. 165-169.
	O2	Shivakumar, P., et al., "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic," *Proceedings of the International Conference on Dependable Systems and Networks*, Washington, D.C., June 23-26, 2002.

Examiner John A. Tarnizo Date Considered 1/26/06

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION CITED BY APPLICANTS THAT MAY BE MATERIAL TO THE PROSECUTION OF THE SUBJECT APPLICATION

Applicants:	Y. Arima et al.	Attorney Docket No.	SUSU121795
Application No.:	10/674,951	Group Art Unit:	2133
Filed:	September 30, 2003	Examiner:	Albert Decady
Title:	INTEGRATED CIRCUIT DEVICE		

FOREIGN PATENT DOCUMENTS

*Examiner Initial	Cite No.	Document No.	Kind Code	Publication Date (mm/dd/yyyy)	Country	English Abstract Provided	Translation Provided
	F3	2002-182803	A	06/28/2002	JP	X	
	F4	2001-350672	A	12/21/2001	JP	X	
	F5	2000-163320	A	06/16/2000	JP	X	
	F6	10-78836	A	03/24/1998	JP	X	
	F7	9-44277	A	02/14/1997	JP	X	
	F8	6-139153	A	05/20/1994	JP	X	
	F9	5-108496	A	04/30/1993	JP	X	

Examiner John P. Trimmer **Date Considered** 1/26/06

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Y. Arima et al. Attorney Docket No.: SUSU121795

Application No.: 10/674,951 Group Art Unit: 2811

Filed: September 30, 2003

Title: INTEGRATED CIRCUIT DEVICE

INFORMATION DISCLOSURE STATEMENT

Seattle, Washington 98101

TO THE COMMISSIONER FOR PATENTS:

Applicants are aware of the information listed in the attached form that may be material to the prosecution of the above-identified patent application.

1. X Copies of the listed publications and other information are enclosed for the Examiner's use.

2. X A concise explanation of the relevance of documents Cites No. F1 and F2 (which are not in the English language), as presently understood by the individual designated under 37 C.F.R. § 1.56(c) most knowledgeable about its content, is provided in the specification of the above-identified application.

3. X Pursuant to 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits.

Respectfully submitted,

CHRISTENSEN O'CONNOR
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Direct Dial No. 206.695.1713

I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date.

Date: 1/8/04

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